ESM00-003

OPAQUE SHIELDING ELEMENT FOR LIQUID CRYSTAL DISPLAY

FIELD OF THE INVENTION

The invention relates in general to an optical element such as a LCD display, and more particularly to an opaque shielding layer for shielding integrated circuit components of the optical element.

BACKGROUND OF THE INVENTION

FIG. 1 is a schematic plan view of a LCD (liquid crystal display) 1 having an array of light valves 2, and row and column addressing lines 3. FIG. 1 shows a 5x5 array of light valves, but typically the LCD display 1 comprises up to 1,200 x 1,000 light valves 2 and associated addressing lines 3. The valves are shown as square arrays but it is to be understood that other shapes, such as rectangles, can be used. In this example, the LCD display is a transmissive type arranged to selectively allow light through the array depending upon the state of each light valve.

FIG. 2 is a schematic cross-sectional view of the LCD display 1. This display optionally comprises upper and lower outer substrates 10 of a suitable transparent

material, such as glass or, for the plate on which the TFT is formed, preferably quartz, at a separation of about 1 to 5mm. The space between the quartz plates 10 is sealed such as by an epoxy sealant (not shown) and filled with a liquid crystal layer 20, suitably a ferroelectric material or a twisted nematic material. Driving circuitry is carried by the plates 10. One of the plates 10 carries a large ,transparent sheet electrode 31 such as indium tin oxide (ITO) that may be coupled to a reference potential such as ground. The other quartz plate 10 carries a driving circuitry layer 30, including a regular array of smaller transparent sheet conductors 2, that define the locations of the pixels of the display, each being connected to a TFT 4 (connections not shown) which is accessed through the row and column addressing lines 3.

In use, a TFT is selectively activated by addressing the row and column addressing lines 3 either from an external circuit or from on-chip control circuitry, in order to change the light transmission properties of the liquid crystal layer 20 in that region, thus forming a light valve corresponding to one pixel of an image.

FIG. 3 is a schematic sectional view of a preferred device structure that may be used in the driving circuitry layer 30. FIG. 3 illustrates two of the TFTs 4 shown in FIG. 2, aid this device structure is repeated many times throughout the circuitry layer 30.

Circuitry sub-structure 30 is shown in greater detail in FIG. 3. Typically, the first layer of the integrated circuitry layer is an active silicon layer 302. The active silicon layer

302 will generally include doped source and drain regions having a channel region between them. Further layers are provided over the active silicon layer 302 in order to form a thin film transistor device as will be apparent to one skilled in the art.

Briefly, the device structure includes the active silicon layer 302, gate oxide 303, gate material 304, insulating layers 305, 306, and 307, surface protection such as oxide layer 309, a black matrix layer 301, positioned to lie between and slightly overlap the pixel areas defined by 2 (see FIG. 2), and conducting layers including a metal 1 (M1) layer 310, and a transparent metal 3 (M3) layer 311 such as indium tin oxide. Layers 311, 310 are connected to 302 and 304 (by connections that are not shown). Alternatively, the black matrix may be positioned on the opposite glass plate (27 in FIG. 2). However, the device structure, per se, is not particularly relevant to the present invention and need not be described in further detail here.

A problem arises in that some portions of the integrated circuitry layer 30, and in particular the active silicon layer 302, are exposed to high intensity visible light radiation (and near ultraviolet radiation) when the optical element is in use, which results in unwanted photoconductivity effects. Hence, it would be advantageous to substantially reduce light intensity in the device structure, especially at the active silicon layer 302.

One application of LCDs for which the above noted photoconductivity effects can be particularly troublesome is to digital projectors. The operation of digital projectors

requires that a very high energy lamp be used. The light is split into three and passed through three displays, one for each color. The three beams are then recombined. Hence there is no color pigmentation included on the LCD itself. The very high energy lamps used in this kind of projector affect the actual transistor performance because of the photoconductivity effects discussed earlier.

Furthermore, the TFT's used in digital projection LCDs are of polysilicon rather than amorphous silicon. The former have much higher mobility and lower leakage currents than the latter. Polysilicon TFTs are manufactured on quartz substrates so that the devices can be processed at temperatures in excess of 1,000EC, compared to amorphous silicon devices which are processed on glass sheets with a maximum processing temperature of about 600EC. This allows the control circuitry to be located on chip as well as allowing much smaller transistors to be fabricated with acceptable leakage.

This invention describes a scheme whereby adding a layer under the TFT's improves immunity to photoconductivity effects.

The black matrix 301 of FIG. 3, or 27 in FIG. 2, is used to block light from between adjacent pixels. In prior art devices it is located on the opposite plate, as shown above. To minimize light scattering across the gap between the plates, it needs to be wider than this gap but this, in turn, reduces the aperture ratio. This is much more of a problem for displays used in digital projectors as the pixel size (15 to 30 microns) is much smaller than

amorphous displays (100 to 200 microns).

A routine search of the prior art was performed with the following references of interest being found:

Kwon et al. in US 5,866,919 and US 5,926,702, show LCDs based on amorphous silicon TFTs, with black matrix layers made of opaque resin located over the active devices on the far side away from the lower plate. US 5,337,068 (Stewart et al.) shows a back-lighted LCD. In US 5,990,999 Yeo shows an LCD with a protective layer. US 6,057,586 (Bawolek et al.) shows a light shielding layer for a light sensor, while US 6,057,896 (Rho et al.) shows a related process. Hsieh et al. (US 5,666,177) show a LCD color display in which there is a black matrix in contact with the lower transparent plate. However, their display contains no TFTs so their black matrix is not a refractory material nor is a lower plate of quartz needed.

SUMMARY OF THE INVENTION

It has been an object of the present invention to provide an optical element wherein components of an included circuitry layer have reduced exposure to strong light intensities during use.

A further object has been that said circuitry layer includes an active silicon layer, and a shielding layer that is between an insulating substrate layer and the active silicon layer.

Another object has been that said optical element be suitable for use in a LCD.

Still another object has been that said LCD be suitable for use as part of a digital projector.

An additional object has been to provide a process for manufacturing said LCD.

These objects have been achieved by inserting an opaque optical shielding element between the TFT active layer and the lower transparent plate of the LCD. By making the lower transparent plate out of quartz, or similar material, and the shielding element from a refractory material such as tungsten, the TFT active layer can be made of polysilicon (as opposed to amorphous silicon) since the plate and shield element will not be affected by the high temperatures, in excess of 1,000 EC, to which they will be exposed when the polysilicon is processed to form TFTs. Optionally, a glue layer may be inserted between the shield layer and the transparent plate and/or the shield elements may be encapsulated within a barrier layer prior to the deposition of the polysilicon. Another option of the present invention is to omit the conventional black matrix, allowing the shielding elements to take

its place.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic plan view of an optical element.

FIG. 2 is a schematic sectional view of the optical element of FIG.1.

FIG. 3 is an more detailed schematic sectional view of part of FIG. 2.

FIG. 4 is a schematic sectional view of a part of FIG. 3, including a thin film transistor below which is an opaque optical shielding element.

FIG. 5 is a closeup view of the shielding element seen in FIG. 4.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to FIG. 4, we show there a more detailed view of TFT 4, first seen in FIG. 2 and again, further expanded into its component parts, in FIG. 3. In a key departure from the prior art, shielding layer 40 is provided between the plate 10 and the circuitry layer 30. By providing the shielding layer 40 on an interior surface of plate 10, good optical register with components of the circuitry layer 30 is assured. Plate 10 may lie toward a

main light receiving direction, illustrated by arrow A in FIG. 4.

It has been difficult to select appropriate materials for the opaque shielding layer 40. It is desired that the shielding layer 40 have good opacity to visible light radiation, as well as to near ultraviolet radiation. Also, the shielding layer should exhibit good planarity and readily receive the device structure of the circuitry layer 30. Its thickness should be between about 0.05 and 1 microns. Further, the initial processing steps in the manufacture of the integrated circuits of the circuitry layer 30 may involve relatively high temperatures. Hence, it is desired that the shielding layer 40 be stable at temperatures in the region of about 600°C to above 1000°C. Additionally, the shielding layer must not degrade the performance of the circuitry layer that is placed on it.

Although metals in general provide the necessary opacity for proper functioning of shielding layer 40, and are easy to deposit, most metals tend to melt during the subsequent high temperature process steps and have been found unsatisfactory in practice. Further still, it is desired that the opaque shielding layer 40 should not contaminate or interfere with the circuitry layer 30, particularly the active silicon layer 302, either during the high temperature processing steps or subsequently.

It has been found that materials suitable for use in the shielding layer 40 include: (a) thermally deposited silicon nitride (b) layers of silicon oxide and silicon nitride, or (c) a refractory metal encapsulated in a suitable barrier layer.

Referring to FIG. 5, in one preferred embodiment the shielding layer 40 comprises a refractory metal layer 41 encapsulated in barrier layer 42. The refractory metal layer 41 suitably comprises tungsten but other metals such as cobalt, titanium, etc. could also have been used or the silicide of a metal such as tungsten could have been used. Optionally, an adhesive layer 43 may also be used. Our preferred material for this has been a titanium/titanium nitride laminate but other similar materials could also have been used. Barrier layer 42 can be a material such as tungsten silicide, tungsten nitride, or titanium nitride or one of these materials could be given an additional cap of deposited silicon oxide, nitride, or oxynitride.

In one preferred fabrication method, the shielding layer 40 is first deposited and patterned on the quartz plate 10, and the active silicon layer 302 of the circuitry layer 30 is formed on the shielding layer. Alternatively, both layers may be patterned simultaneously. This is followed by the formation of wiring layer 310. In all cases, the shielding layer 40 forms a regular array of transparent portions divided by non-transparent shielded portions. Further, the non-transparent portions are aligned in good optical register with the sections of the circuitry layer 30 that it is desired to shield from optical radiation. In particular, excellent optical alignment with the active silicon layer 302 is possible.

The shielding layer 40 may comprise a reflective material that scatters light back toward the light source, or it may comprise a non-reflective light absorbent material. Where

a non-reflective material is used it is desirable that this material be a relatively good thermal conductor, and that the shielding layer 40 be thermally coupled to a heat sink. Another option is to allow the shielding elements to provide the function of the black matrix.

Three particular examples will now be described to illustrate the preferred embodiments of the present invention.

Silicon nitride can be deposited on an underlying substrate using either Plasma Enhanced Chemical Vapor Deposition (PECVD) or a Low Pressure Chemical Vapor Deposition (LPCVD) process. Typically LPCVD silicon nitride is deposited using either a DCS/NH_3 or SiH_4/NH_3 gas source at between 700-850 EC. A typical PECVD silicon nitride is deposited using a combination of $SiH_4/N_2O/NH_3$ gas sources at between 300-400 EC .

Silicon dioxide (SiO_2) can either be grown or deposited on the underlying substrate. Silicon dioxide can be thermally grown on a silicon substrate using either a dry oxidation (O_2 only) or a wet oxidation ($H_2O_2+O_2$) at temperatures typically between 800-1100 EC. In the case of deposited oxides, techniques such as PECVD, LPCVD or Atmospheric Pressure Chemical Vapor Deposition (APCVD) can be used. PECVD would typically use a SiH_4 gas source at temperatures between 300-400 EC. LPCVD uses $TEOS/O_2$ at temperatures of 600-800 EC, or SiH_4 /O_2 at lower temperatures. APCVD would use a SiH_4/O_2 gas source at temperatures between 350-500 EC.